What is claimed is:

1. A semiconductor device comprising at least one defect-free epitaxial layer, wherein at least a part of the device is manufactured by a method of fabrication of defect–free epitaxial layers on top of a surface of a first solid state material having a first thermal evaporation rate and a plurality of defects, wherein the surface comprises at least one defect-free surface region, and at least one surface region in a vicinity of the defects, the method comprising the steps of:

a) depositing a cap layer comprising a second material having a second thermal evaporation rate different from the first thermal evaporation rate, wherein the cap layer is selectively deposited on the defect–free surface region, such that at least one of the regions of the surface in the vicinity of the defects remains uncovered;

b) annealing a structure created in step a) at a temperature and duration such that at least one of the surface regions in the vicinity of the defects that is uncovered evaporates, while defect-free surface regions covered by the cap layer remain unaffected, and at least one annealed region is formed; and

c) depositing a third material, lattice–matched or nearly lattice matched to the first solid state material, such that the third material overgrows both the cap layer and annealed regions of the first solid state material forming a defect-free epitaxial layer.

2. The semiconductor device of claim 1, wherein the device is selected from the group consisting of:

a) a high electron mobility transistor;

b) a field effect transistor;

c) a heterojunction bipolar transistor; and

d) an integrated circuit.

3. The semiconductor device of claim 1, wherein the device is selected from the group consisting of:

a) a diode laser;

b) a light-emitting diode;

c) a photodetector;

d) an optical amplifier;

e) a far infrared intraband detector;

f) an intraband far infrared emitter;

g) a resonant tunneling diode;

h) a solar cell; and

i) an optically bistable device.

4. The semiconductor device of claim 1, wherein the device is selected from the group consisting of:

a) a current-injection edge-emitting laser;

b) a vertical cavity surface emitting laser; and

c) a tilted cavity laser.

5. The semiconductor device of claim 1, wherein the first solid state material is selected from the group consisting of:

a) a defect–containing substrate; and

b) a defect–containing epitaxial layer.

6. The semiconductor device of claim 1, wherein at least one defect is a propagating defect selected from the group consisting of:

a) at least one threading dislocation;

b) at least one screw dislocation;

c) at least one stacking fault;

d) at least one antiphase boundary; and

e) any combination of a) through d).

7. The semiconductor device of claim 1, wherein the defects comprise at least one local defect which causes a propagating defect in a subsequently deposited epitaxial layer.

8. The semiconductor device of claim 7, wherein the local defect is selected from the group consisting of:

a) at least one local dislocation;

b) at least one misfit dislocation;

c) at least one local defect dipole;

d) at least one dislocation network;

e) at least one dislocation loop;

f) at least one dislocated cluster;

g) at least one impurity precipitate;

h) at least one oval defect;

i) a plurality of dirt particles on the surface; and

j) any combination of a) through i).

9. The semiconductor device of claim 1, wherein step (a) of the method comprises a deposition process selected from the group consisting of:

a) molecular beam epitaxy deposition;

b) metal-organic chemical vapor deposition; and

c) vapor phase epitaxy deposition.

10. The semiconductor device of claim 1, wherein step (c) of the method comprises a deposition process selected from the group consisting of:

a) molecular beam epitaxy deposition;

b) metal-organic chemical vapor deposition; and

c) vapor phase epitaxy deposition.

11. The semiconductor device of claim 1, wherein steps (a) and (b) of the method are repeated two times to twenty times.

12. The semiconductor device of claim 1, wherein steps (a) through (c) of the method are repeated two times to forty times.

13. The semiconductor device of claim 1, wherein the surface region in the vicinity of the defects differs from the defect-free surface region in a strain state, such that the cap layer is repelled from and does not cover the surface region in the vicinity of the defects.

14. The semiconductor device of claim 1, wherein the surface region in the vicinity of the defects differs from the defect-free surface region in a surface energy, such that the cap layer is repelled from and does not cover the surface region in the vicinity of the defects.

15. The semiconductor device of claim 1, wherein the surface region in the vicinity of the defects differs from the defect-free surface region in a surface stress, such that the cap layer is repelled from and does not cover the surface region in the vicinity of the defects.

16. The semiconductor device of claim 1, wherein the surface region in the vicinity of the defects differs from the defect-free surface region in a surface morphology, such that the cap layer is repelled from and does not cover the surface region in the vicinity of the defects.

17. The semiconductor device of claim 1, wherein the surface region in the vicinity of the defects differs from the defect-free surface region in wetting/non-wetting properties with respect to the deposition of the cap layer material, such that the cap layer is repelled from and does not cover the surface region in the vicinity of the defects.

18. The semiconductor device of claim 1, wherein an evaporation of the defect-containing regions is enhanced by chemical etching using a flux of chemically–active particles, wherein the chemically–active particles are selected from the group consisting of:

a) atoms;

b) molecules; and

c) ions.

19. The semiconductor device of claim 1, wherein an evaporation of the defect-containing regions is enhanced by a plasma etching process.

20. The semiconductor device of claim 1, wherein an evaporation of the defect-containing regions is enhanced by a wet etching process.

21. The semiconductor device of claim 1, wherein the thermal annealing in step (b) of the method results in the formation of troughs at a plurality of exits of the defects in the first solid state material.

22. The semiconductor device of claim 1, wherein the growth of the second epitaxial layer occurs in the lateral epitaxial overgrowth mode.

23. The semiconductor device of claim 22, wherein step (c) of the method comprises the substeps of:

a) starting growth of the third material at the surface regions covered by the cap layer;

b) continuing the growth of the third material in a lateral plane resulting in merging of neighboring domains of lateral epitaxial overgrowth; and

c) forming the defect-free epitaxial layer from the third material, wherein the defect-free epitaxial layer is suitable for further epitaxial growth.

24. The semiconductor device of claim 1, wherein at least one void remains in the third material.

25. The semiconductor device of claim 1, wherein no voids remain in the third material.

26. The semiconductor device of claim 1, wherein the method further comprises the step of, prior to step (a), the deposition of a fourth material, lattice–matched or nearly lattice–matched to the first solid state material, wherein the fourth material provides a repulsion of the second material of the cap layer from defect-containing surface regions.

27. The semiconductor device of claim 1, wherein the method further comprises the step of, prior to step (a), the deposition of a fourth material, wherein the fourth material is in a no-strain state lattice–mismatched to the first solid state material, wherein a thickness of the fourth material is below a critical thickness required for a creation of new defects, such that the fourth material forms a strained defect-free thin pseudomorphic layer.

28. The semiconductor device of claim 27, wherein the pseudomorphic layer provides a repulsion of the second material of the cap layer from defect-containing surface regions.

29. A semiconductor device comprising at least one defect-free epitaxial layer, wherein at least a part of the device is manufactured by a method of fabrication of defect–free

epitaxial layers on a surface of a defect–containing first epitaxial layer, the method comprising the steps of:

a) depositing the first epitaxial layer having a first thermal evaporation rate, wherein the first epitaxial layer is lattice-mismatched to a substrate, wherein a thickness of the first epitaxial layer exceeds a critical thickness required for a formation of defects, such that a plurality of defects are formed in the first epitaxial layer, wherein the surface of the first epitaxial layer comprises at least one defect-free surface region, and at least one surface region in a vicinity of the defects;

b) depositing a cap layer of a second material having a second thermal evaporation rate different from the first thermal evaporation rate, such that the cap layer is selectively deposited on the defect–free surface regions, and at least one of the surface regions in the vicinity of the defects remains uncovered;

c) annealing a structure formed in step b) at a temperature and duration such that at least one of the surface regions in the vicinity of the defects that is uncovered evaporates, while defect-free surface regions covered by the cap layer remain unaffected, and at least one annealed region is formed; and

d) depositing a third material, lattice–matched or nearly lattice matched to the first epitaxial layer, such that the third material overgrows both the cap layer and annealed regions of the first epitaxial layer, forming a defect-free epitaxial layer suitable as a template for further epitaxial growth.

30. A high electron mobility transistor comprising:

a) a substrate selected from the group consisting of a Si substrate and a GaAs substrate;

b) a plastically relaxed $Ga_{1-x}In_xAs$ layer grown on top of the substrate; and

c) a defect–free $Ga_{1-y}In_yAs$ layer grown on top of the plastically relaxed layer.

31. A high electron mobility transistor comprising:

a) a substrate selected from the group consisting of a Si substrate and a GaAs substrate;

b) a plastically relaxed $Ga_{1-x}In_xAs$ layer grown on top of the substrate; and

c) a defect–free $Ga_{1-y-z}In_yAl_zAs$ layer grown on top of the plastically relaxed $Ga_{1-x}In_xAs$ layer.

32. A high electron mobility transistor comprising:

a) a substrate selected from the group consisting of a Si substrate with a surface orientation (111), a SiC substrate, and a sapphire substrate;

b) a plastically relaxed GaN layer grown on top of the substrate; and

c) a defect–free GaN layer grown on top of the plastically relaxed GaN layer.

33. A high electron mobility transistor comprising:

a) a substrate selected from the group consisting of a Si substrate with a surface orientation (111), a SiC substrate, and a sapphire substrate;

b) a plastically relaxed $Ga_{1-x}In_xN$ layer grown on top of the substrate; and

c) a defect–free $Ga_{1-y}In_yN$ layer grown on top of the plastically relaxed $Ga_{1-x}In_xN$ layer.

34. An integrated circuit comprising:

a) a Si substrate;

b) a plastically relaxed $Si_{1-x}Ge_x$ layer grown on top of the Si substrate;

c) a defect–free $Si_{1-y}Ge_y$ layer grown on top of the plastically relaxed $Si_{1-x}Ge_x$ layer; and

d) a thin pseudomorphically strained Si layer grown on top of the defect–free $Si_{1-y}Ge_y$ layer.

35. A tilted cavity laser grown on an GaAs substrate, wherein an n-part of a cavity comprises:

a) an epitaxial layer comprising a material selected from the group consisting of GaAs and $Ga_{1-z}Al_zAs$;

b) a plastically relaxed $Ga_{1-x}In_xAs$ layer grown on top of the epitaxial layer; and

c) a defect-free $Ga_{1-y}In_yAs$ layer grown on top of the plastically relaxed $Ga_{1-x}In_xAs$ layer.

36. The tilted cavity laser of claim 117, wherein the laser generates laser light in the wavelength region of 1.4 through 1.8 micrometers.

37. A GaN-based vertical cavity surface emitting laser comprising a cavity, wherein at least a part of the cavity is made by a method comprising the steps of:

a) depositing a first epitaxial layer having a first thermal evaporation rate on a substrate, wherein the first epitaxial layer is lattice-mismatched to the substrate, wherein a thickness of the first epitaxial layer exceeds a critical thickness required for a formation of defects, such that a plurality of defects are formed in the first epitaxial layer, such that a surface of said first epitaxial layer comprises at least one defect-free surface region, and at least one surface region in a vicinity of the defects;

b) depositing a cap layer of a second material having a second thermal evaporation rate different from the first thermal evaporation rate, such that the cap layer is selectively deposited on the defect–free surface regions, and at least one of the surface regions in the vicinity of the defects remains uncovered;

c) annealing a structure formed in step b) at a temperature and duration such that at least one of the surface regions in the vicinity of the defects that is

uncovered evaporates, while defect-free surface regions covered by the cap layer remain unaffected, and at least one annealed region is formed; and

d) depositing a third material, lattice–matched or nearly lattice matched to the first epitaxial layer, such that the third material overgrows both the cap layer and annealed regions of the first epitaxial layer, forming a defect-free epitaxial layer suitable as a template for further epitaxial growth.

38. The GaN-based vertical cavity surface emitting laser of claim 37, wherein the laser generates laser light in a wavelength region from 100 nanometers to 600 nanometers.

39. A GaN-based edge-emitting laser comprising a waveguide, wherein at least a part of the waveguide is made by a method comprising the steps of:

a) depositing a first epitaxial layer having a first thermal evaporation rate on a substrate, wherein the first epitaxial layer is lattice-mismatched to the substrate, wherein a thickness of the first epitaxial layer exceeds a critical thickness required for a formation of defects, such that a plurality of defects are formed in the first epitaxial layer, such that a surface of said first epitaxial layer comprises at least one defect-free surface region, and at least one surface region in a vicinity of the defects;

b) depositing a cap layer of a second material having a second thermal evaporation rate different from the first thermal evaporation rate, such that the cap layer is selectively deposited on the defect–free surface regions, and at least one of the surface regions in the vicinity of the defects remains uncovered;

c) annealing a structure formed in step b) at a temperature and duration such that at least one of the surface regions in the vicinity of the defects that is uncovered evaporates, while defect-free surface regions covered by the cap layer remain unaffected, and at least one annealed region is formed; and

d) depositing a third material, lattice–matched or nearly lattice matched to the first epitaxial layer, such that the third material overgrows both the cap layer

and annealed regions of the first epitaxial layer, forming a defect-free epitaxial layer suitable as a template for further epitaxial growth.

40. The GaN-based edge-emitting laser of claim 39, wherein the laser generates laser light in a wavelength region from 100 nanometers to 600 nanometers.

41. A GaN-based tilted cavity laser comprising a cavity, wherein at least a part of the cavity is made by a method comprising the steps of:

a) depositing a first epitaxial layer having a first thermal evaporation rate on a substrate, wherein the first epitaxial layer is lattice-mismatched to the substrate, wherein a thickness of the first epitaxial layer exceeds a critical thickness required for a formation of defects, such that a plurality of defects are formed in the first epitaxial layer, such that a surface of said first epitaxial layer comprises at least one defect-free surface region, and at least one surface region in a vicinity of the defects;

b) depositing a cap layer of a second material having a second thermal evaporation rate different from the first thermal evaporation rate, such that the cap layer is selectively deposited on the defect–free surface regions, and at least one of the surface regions in the vicinity of the defects remains uncovered;

c) annealing a structure formed in step b) at a temperature and duration such that at least one of the surface regions in the vicinity of the defects that is uncovered evaporates, while defect-free surface regions covered by the cap layer remain unaffected, and at least one annealed region is formed; and

d) depositing a third material, lattice–matched or nearly lattice matched to the first epitaxial layer, such that the third material overgrows both the cap layer and annealed regions of the first epitaxial layer, forming a defect-free epitaxial layer suitable as a template for further epitaxial growth.

42. The GaN-based tilted cavity laser of claim 41, wherein the laser generates laser light in the wavelength region from 100 nanometers to 600 nanometers.